What is claimed is:

1. A delay-locked loop for receiving an external clock signal and synchronizing a phase of a feedback clock signal with a phase of the external clock signal, the delay-locked loop comprising:

a phase detector for comparing the phase of the external clock signal with the phase of the feedback clock signal and outputting a phase difference as an error control signal;

a delay line, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a predetermined shift signal; and

a filter unit for generating the shift signal for selecting the number of delay cells in operation in the delay line, in response to the error control signal.

2. The delay-locked loop of claim 1, wherein the delay line is structured such that a unit time delay gradually increases from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

3. The delay-locked loop of claim 1, wherein each delay cell is a differential amplifier and adjusts a resistance connected to a power supply voltage to vary the unit time delay.

4. The delay-locked loop of claim 3, wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

5. The delay-locked loop of claim 3, wherein the differential amplifier comprises an input transistor, to which the external clock signal is transmitted, having a size that gradually increases from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

6. The delay-locked loop of claim 3, wherein the differential amplifier includes a capacitor at an output end,

wherein a capacitance of the capacitor gradually increases from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

7. A synchronous mirror delay comprising:

a forward delay array (FDA), comprising a plurality of delay cells having various unit time delays, for receiving an external clock signal and generating a forward delay clock signal by forward delaying a phase of the external clock signal;

a mirror control circuit for delaying and outputting the forward delay clock signal in response to the forward delay clock signal and the external clock signal; and

a backward delay array (BDA), comprising a plurality of serially connected delay cells having various unit time delays, for receiving an output of the mirror control circuit and generating a backward delay clock signal by backward delaying a phase of an output of the mirror control circuit.

8. The synchronous mirror delay of claim 7, wherein the plurality delay cells of the forward delay array and backward delay array have unit time delays that gradually increased from the delay cell of a front end of the respective array to the delay cell of a rear end of the respective array.

9. The synchronous mirror delay of claim 7, wherein each delay cell comprises a NAND gate and an inverter that are connected in series, and wherein the unit time delay is varied according to the sizes of the transistors of the NAND gate and the inverter.

10. The synchronous mirror delay of claim 9, wherein a size of the transistor is gradually increased from the delay cell at a front end of the array to the delay cell at a rear end of the array, wherein the array is at least one of the forward delay array and the backward delay array.

11. The synchronous mirror delay of claim 9, wherein each delay cell comprises a capacitor at an output end,

and wherein the capacitance of the capacitor gradually increases from the delay cell at the front end of the array to the delay cell at the rear end of the array,

wherein the array is at least one of the forward delay array and the backward delay array.

12. The synchronous mirror delay of claim 7, wherein the forward delay array and the backward delay array comprise even-numbered delay cells have longer unit time delays than odd-numbered delay cells.

13. The synchronous mirror delay of claim 7, wherein the forward delay array and the backward delay array comprise odd-numbered delay cells have longer unit time delays than even-numbered delay cells.

14. A time delay compensation circuit for synchronizes an output clock signal with an external clock signal, the time delay compensation circuit comprising:

a delay unit, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal and generating the output clock signal in synchronization with the external clock signal; and

a control unit for selecting a number of delay cells in the delay unit and controlling the number of delay cells in operation such that the output clock signal is synchronized with the external clock signal.

15. The circuit of claim 14, wherein the delay cells of the delay unit have gradually increasing unit time delays from the delay cell at the front end of the delay unit to the delay cell at the rear end of the delay unit.

16. The circuit of claim 14, wherein the delay unit comprises even-numbered delay cells having longer unit time delays than odd-numbered delay cells.

17. The circuit of claim 14, wherein the delay unit comprises odd-numbered delay cells have longer unit time delays than even-numbered delay cells.